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PATENT
068167.0107

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Giles, et al.

Serial No.: 09/809,731

Filed: March 15, 2001

Invention: Method for Hybrid Processing of
Software Instructions of an
Emulated Computer System

Commissioner for Patents
Washington, D.C. 20231

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Group No.: 2132

Examiner: Not Yet Assigned

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Applicant respectfully requests, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner. Pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

The information disclosure statement submitted herewith is being submitted before the mailing of the first office action on the merits. Applicants believe that no fee is required. If a fee is required, please charge any fee to Deposit Account No. 02-0383 of Baker Botts L.L.P.

Respectfully submitted,



Roger Fulghum
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(713) 229-1707
Attorney Docket No.: 068167.0107

Date: March 6, 2002

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Pursuant to 37 C.F.R. § 1.8, I hereby certify that I have information and a reasonable basis for belief that this correspondence will be deposited as first-class mail with the United States Postal Service in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231 on April 3, 2002.

K. E. J. R.
Signature

4-3-02
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Giles, et al.

Serial No.: 09/809,731

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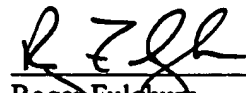
Technology Center 2100

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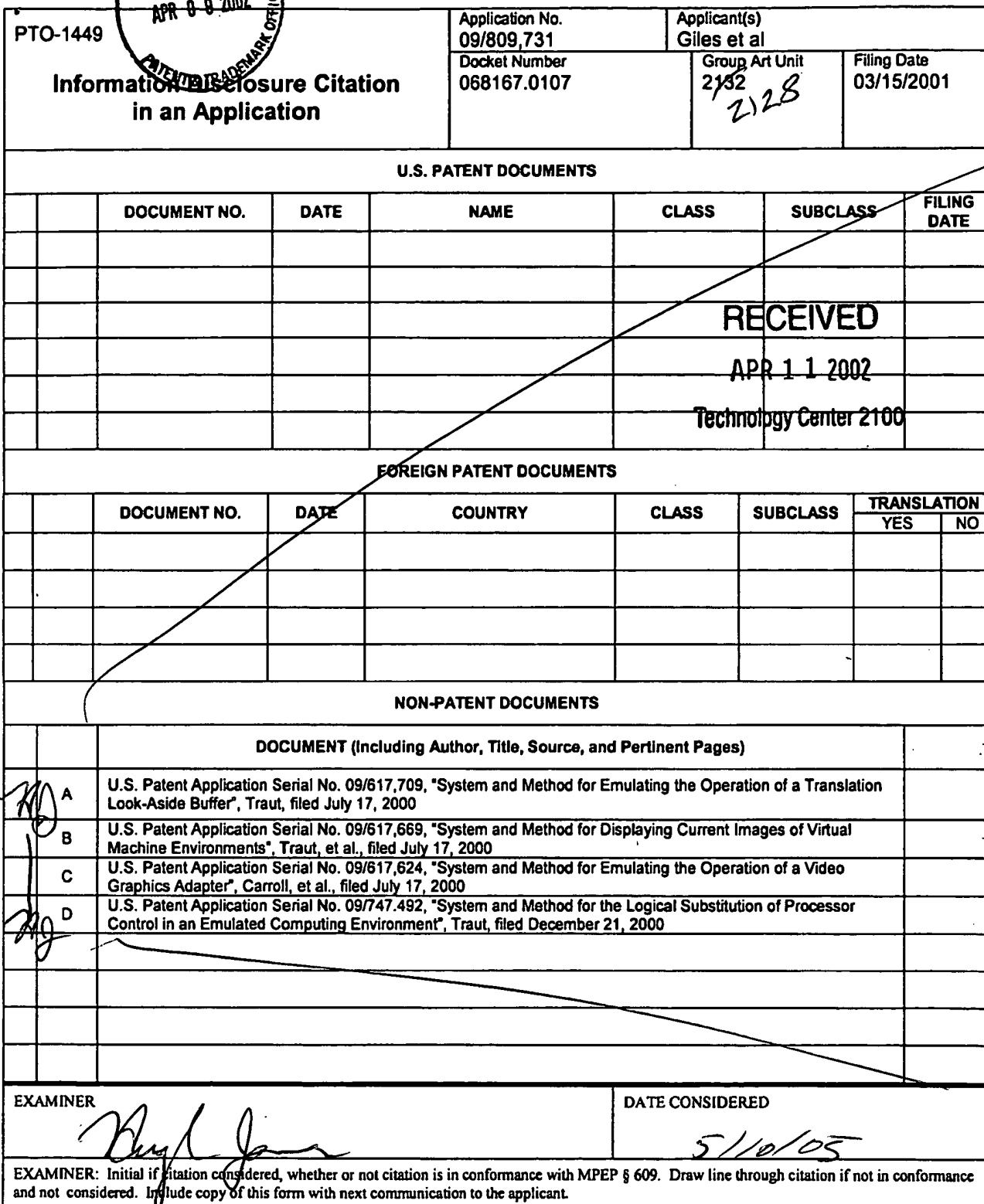
Respectfully submitted,

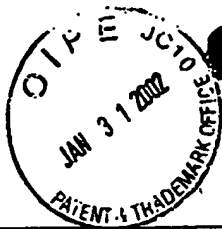


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Date: April 3, 2002





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PATENT
068167.0107

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Pursuant to 37 C.F.R. § 1.8, I hereby certify that I have information and a reasonable basis for belief that this correspondence will be deposited as first-class mail with the United States Postal Service in an envelope addressed to the Commissioner for Patents, Washington, D.C. 20231.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

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Serial No.: 09/809,731

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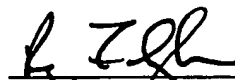
Examiner: Not Yet Assigned

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

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Attorney Docket No.: 068167.0107

Date: January 17, 2002

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PTO-1449

Application No.
09/809,731

Applicant(s)
Giles, et al.

Docket Number
068167.0107

Group Art Unit
2132
2128

Filing Date
3/15/01

**Information Disclosure Citation
in an Application**

U.S. PATENT DOCUMENTS

	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
A	5278973	1/11/94	O'Brien et al.	395	500	6/27/91
B	5301277	4/5/94	Kanai	709	301	12/23/91
C	5367628	11/22/94	Ote et al.	345	501	10/15/92
D	5448264	9/5/95	Pinedo et al.	345	508	6/14/93
E	5452456	9/19/95	Mourey et al.	713	100	12/18/92
F	5502809	3/26/96	Takano	345	509	9/6/94
G	5640562	6/17/97	Wold et al.	395	652	2/27/95
H	5666521	9/9/97	Marisetty	345	525	11/20/96
I	5742797	4/21/98	Celi, Jr. et al.	345	507	8/11/95
J	5752275	5/12/98	Hammond	711	207	7/14/97
K	5757386	5/26/98	Celi, Jr. et al.	345	507	8/11/95
L	5790825	8/4/98	Traut	712	209	8/5/97
M	5831607	11/3/98	Brooks	345	333	1/25/96
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O	5940872	8/17/99	Hammond et al.	711	207	11/1/96
P	6014170	1/11/00	Pont et al.	348	232	6/20/97
Q	6026476	2/15/00	Rosen	711	206	8/6/97
R	6067618	5/23/00	Weber	713	1	3/26/98

FOREIGN PATENT DOCUMENTS

DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO

NON-PATENT DOCUMENTS

DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	
S "Processor Instruction Sets," The PC Guide, version date 12/18/00, http://www.pcguide.com/ref/cpu/arch/int/inst-c.html .	
T "M68060 User's Manual," Motorola, 1994, pp. i-xviii; Section 4, Memory Management Unit, pp. 4-1 to 4-30, http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/68K-COLDFIRE/M680X0/MC68060UM.pdf .	
U "MPC750, RISC Microprocessor User's Manual," Motorola, 8/97, Contents, pp. iii-xvi; Chapter 5, Memory Management, pp. 5-1 to 5-34; Glossary, pp. Glossary-1 to Glossary-13, http://e-www.motorola.com/brdata/PDFDB/MICROPROCESSORS/32_BIT/POWERPC/MPC7XX/MPC750UM.pdf .	

EXAMINER

DATE CONSIDERED

[Signature]

5/10/05

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[Signature]
Signature

3-27-02
Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Giles, et al.

Serial No.: 09/809,731

Filed: March 15, 2001

Invention: Method for Hybrid Processing of
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Emulated Computer System

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Group No.: 2132

Examiner: Not Yet Assigned


Commissioner for Patents
Washington, D.C. 20231

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Attorney Docket No.: 068167.0107

Date: March 27, 2002



#7

PTO-1449		Application No. 09/809,731		Applicant(s) Giles, et al.				
Information Disclosure Citation in an Application		Docket Number 068167.0107		Group/Art Unit 2132 2128	Filing Date 3/15/01			
U.S. PATENT DOCUMENTS								
		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
<input checked="" type="checkbox"/>	A	5,815,686	9/29/98	Earl, et al.	395	500	9/12/96	
<input checked="" type="checkbox"/>	B	4,779,188	10/18/88	Gum et al.	364	200	10/19/87	
FOREIGN PATENT DOCUMENTS								
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
<input checked="" type="checkbox"/>	C	EP 0 645 701 A2	26/09/94	EPO	G06F	9/455	X	
NON-PATENT DOCUMENTS								
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)						
<input checked="" type="checkbox"/>	D	PCT International Search Report in International Application No. PCT/US 01/22276, International filing date 16/07/01, mail date 07/03/02.						
<input checked="" type="checkbox"/>	E	Traut E, "Building the Virtual PC," Byte, McGraw-Hill Inc., Vol. 22, No. 11, pp. 51-52, 1 November 1997.						
<input checked="" type="checkbox"/>	F	"Intel386 DX Microprocessor," Intel, pp. 32-58, 31 December 1995.						
<input checked="" type="checkbox"/>	G	"Macintosh and Technology: Changing Chips in the Middle of the Stream, or Apple Takes a Risc," URL: www.btech.co/changingchips.html, paragraphs '00061-'00071, retrieved 12/10/01.						
<input checked="" type="checkbox"/>	H	"M68040 User's Manual," Motorola, Inc., Chapter 3, copyright 1990, revised 1992, 1993.						
<input checked="" type="checkbox"/>	I	Osisek DL et al., "ESA/390 Interpretive-Execution Architecture, Foundation for VM/ESA," IBM Systems Journal, Vol. 30, No. 1, pp. 34-51, 1991.						
<input checked="" type="checkbox"/>	J	Shang Rong Tsai et al., "On the Architectural Support for Logical Machine Systems," Microprocessing and Microprogramming, Vol. 22, No. 2, pp. 81-96, February 1988.						
EXAMINER 					DATE CONSIDERED 5/10/05			
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